

IN THE CLAIMS:

Please amend claims 36, 39, 40, 44-49 and 51-52; and cancel claims 37-38 and 50, as set forth below:

1-35. (Canceled)

36. (Currently amended) A pFET synapse transistor, comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including: [[:]]

a first n- well ~~and a second n- well disposed in said p- doped substrate;~~

a first p+ doped region disposed in said first n- well forming a first source; ~~and~~

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased responsive to increase in a voltage difference between the first source and the first drain; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, a number of electrons removed from the second polysilicon floating gate increase responsive to increase in voltage at the second drain or the second source.

~~a third p+ doped region and a fourth p+ doped region disposed in said second n-well, said third p+ doped region and said fourth p+ doped region together forming a tunneling junction;~~

~~a layer of gate oxide disposed above said channel, said first n-well and said second n-well;~~

~~a polysilicon floating gate disposed above said layer of gate oxide;~~

~~a source contact terminal electrically coupled to said source;~~

~~a drain contact terminal electrically coupled to said drain; and~~

~~a well contact terminal electrically coupled to said second n-well.~~

37-38. (Canceled)

39. (Currently amended) [[A]] The pFET synapse transistor in accordance with claim 36
~~claim 38, wherein said readout transistor and the shorted transistor include transistor is~~
~~formed with~~ a single layer of conductive polysilicon.

40. (Currently amended) [[A]] The pFET synapse transistor in accordance with claim 36
fabricated using a standard CMOS process.

41-43. (Canceled)

44. (Currently amended) A pFET synapse transistor, comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including: [[:]]

a first n- well ~~and a second n- well disposed in said substrate;~~

a first p+ doped region disposed in said first n- well forming a first source; and

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased responsive to increase in a voltage difference between the first source and the first drain; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate;

a conductor connecting the second drain and the second source, a number of
electrons removed from the second polysilicon floating gate increased responsive to
increase in voltage at the second drain or the second source; and
~~a third p+ doped region and a fourth p+ doped region disposed in said second n- well,~~
~~said third p+ region and said fourth p+ region together forming a tunneling junction;~~
~~a layer of gate oxide disposed above said channel, said first n- well and said second n-~~
~~well;~~
~~a polysilicon floating gate disposed above said layer of gate oxide;~~
~~a source contact terminal electrically coupled to said source;~~
~~a drain contact terminal electrically coupled to said drain; and~~
 a well contact terminal electrically coupled to said second n- well, wherein
 said synapse transistor is configured to operate as a current source without gate input
 using a single polysilicon gate layer.

45. (Currently amended) A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

a pFET synapse transistor including:

a readout transistor for injecting electrons into a floating gate, the readout
transistor comprising:

a p- doped substrate including;

a first n- well ~~and a second n- well disposed in said p-~~
~~doped substrate;~~

a first p+ doped region disposed in said first n- well
 forming a first source; ~~and~~

a second p⁺ doped region disposed in said first n- well
forming a first drain, a number of electrons injected into the
floating gate increased responsive to increase in a voltage
difference between the first source and the first drain; and
a channel disposed in said first n- well between said
source and said drain;
a first layer of gate oxide above said channel and said first n- well; and
a first polysilicon floating gate disposed above said layer of gate
oxide; and
a shorted transistor for removing electrons from the floating gate, the shorted
transistor comprising:
a p- doped substrate including a second n-well, a second drain within
the second n-well, and a second source within the second n-well;
a second layer of gate oxide above said first n- well;
a second polysilicon floating gate above said second layer of gate
oxide, the second polysilicon floating gate connected to the first polysilicon
floating gate; and
a conductor connecting the second drain and the second source, a
number of electrons removed from the second polysilicon floating gate
increased responsive to increase in voltage at the second drain or the second
source.

~~a third p⁺ doped region and a fourth p⁺ doped region disposed in said second n- well,~~
~~said third p⁺ region and said fourth p⁺ region together forming a tunneling junction;~~

~~a layer of gate oxide disposed above said channel, said first n-well and said second n-well;~~

~~a polysilicon floating gate disposed above said layer of gate oxide;~~

~~a source contact terminal electrically coupled to said source;~~

~~a drain contact terminal electrically coupled to said drain; and~~

~~a well contact terminal electrically coupled to said second n-well.~~

46. (Currently amended) A p-channel floating-gate device, comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p-doped substrate including: [[:]]

a first n-well ~~and a second n-well~~ disposed in said p-doped substrate;

a first p⁺ doped region disposed in said first n-well forming a first source; ~~and~~

a second p⁺ doped region disposed in said first n-well forming a first drain, a number of electrons injected into the floating gate increased responsive to increase in a voltage difference between the first source and the first drain; and

a channel disposed in said first n-well between said source and said drain;

a first layer of gate oxide above said channel and said first n-well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, a number of electrons removed from the second polysilicon floating gate increased responsive to increase in voltage at the second drain or the second source.

~~a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;~~

~~a layer of gate oxide disposed above said channel, said first n- well and said second n- well;~~

~~a single polysilicon layer disposed above said layer of gate oxide, said single polysilicon layer comprising a floating gate;~~

~~a source contact terminal electrically coupled to said source;~~

~~a drain contact terminal electrically coupled to said drain; and~~

~~a well contact terminal electrically coupled to said second n- well.~~

47. (Currently amended) A system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip, the system comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including: [[:]]

a first n- well and ~~a second n- well~~ disposed in said p- doped substrate;

a first p+ doped region disposed in said first n- well forming a first source; ~~and~~

a second p+ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased responsive to increase in a voltage difference between the first source and the first drain; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and

a first polysilicon floating gate disposed above said layer of gate oxide; and

a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:

a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well;

a second layer of gate oxide above said first n- well;

a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and

a conductor connecting the second drain and the second source, a number of electrons removed from the second polysilicon floating gate increased responsive to increase in voltage at the second drain or the second source.

~~a third p⁺ doped region and a fourth p⁺ doped region disposed in said second n-well,
said third p⁺ region and said fourth p⁺ region together forming a tunneling junction;~~

~~a layer of gate oxide disposed above said channel, said first n-well and said second n-well;~~

~~a single polysilicon layer disposed above said layer of gate oxide, said single polysilicon layer comprising a floating gate;~~

~~a source contact terminal electrically coupled to said source;~~

~~a drain contact terminal electrically coupled to said drain; and~~

~~a well contact terminal electrically coupled to said second n-well.~~

48. (Currently amended) A p-channel floating gate device comprising:

a readout transistor for injecting electrons into a floating gate, the readout transistor comprising:

a p- doped substrate including: [[:]]

~~a first n- well and a second n-well disposed in said p- doped substrate;~~

a first p⁺ doped region disposed in said first n- well forming a first source; ~~and~~

a second p⁺ doped region disposed in said first n- well forming a first drain, a number of electrons injected into the floating gate increased responsive to increase in a voltage difference between the first source and the first drain; and

a channel disposed in said first n- well between said source and said drain;

a first layer of gate oxide above said channel and said first n- well; and
a first polysilicon floating gate disposed above said layer of gate oxide; and
a shorted transistor for removing electrons from the floating gate, the shorted transistor comprising:
a p- doped substrate including a second n-well, a second drain within the second n-well, and a second source within the second n-well;
a second layer of gate oxide above said first n- well;
a second polysilicon floating gate above said second layer of gate oxide, the second polysilicon floating gate connected to the first polysilicon floating gate; and
a conductor connecting the second drain and the second source, a number of electrons removed from the second polysilicon floating gate increased responsive to increase in voltage at the second drain or the second source.
~~a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ region and said fourth p+ region together forming a tunneling junction;~~
~~a layer of gate oxide disposed above said channel, said first n- well and said second n- well;~~
~~a polysilicon floating gate disposed above said layer of gate oxide;~~
~~a source contact terminal electrically coupled to said source;~~
~~a drain contact terminal electrically coupled to said drain; and~~
~~a well contact terminal electrically coupled to said second n- well.~~

49. (Currently amended) [[A]] p-channel floating gate device in accordance with claim 48, wherein the second drain comprises a said third p+ doped region within the second n- well, the second source comprises a and said fourth p+ doped region, wherein the conductor

~~comprises~~ ~~are shorted together with~~ a conductive layer which forms a bridge over said second polysilicon floating gate.

50. (Canceled)

51. (Currently amended) [[A]] The p-channel floating gate device in accordance with claim 48 ~~claim 50~~, wherein said readout transistor and the shorted transistor include transistor ~~is formed with~~ a single layer of conductive polysilicon.

52. (Currently amended) [[A]] The p-channel floating gate device in accordance with claim 48, wherein the floating gate device is fabricated using a standard CMOS process.